REMARKS

Claims 1-4, 6, 9, 20, and 23-30 are presently pending in the application. Claims 5, 7, 8, 10-19, 21, and 22 previously were canceled without prejudice or disclaimer as being directed to non-elected inventions. Claims 1 and 9 have been amended to define more clearly the features of the present invention. Claims 23-30 have been added to provide more varied protection for the present invention.

It is noted that the claim amendments are made only for canceling non-elected claims, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claim 20 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Damouny (U.S. Patent No. 4,713,750). Claims 1-4, 6, and 9 stand rejected under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma (U.S. Patent No. 4,484,268).

These rejections are respectfully traversed in the following discussion.

I. THE PRESENT INVENTION

The claimed invention relates to a microprocessor, a microcode unit in a microprocessor, and a method of providing a state machine decoding.

In the illustrative, non-limiting embodiment of the invention, as defined by independent claim 1, a microprocessor includes a microcode unit for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions. The microcode unit includes an instruction address input for receiving an instruction address, a

control variable input for receiving a control variable corresponding to a current state of the microprocessor, a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction, and a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals *required* for executing said received instruction.

In another exemplary embodiment of the present invention, as defined by independent claim 9, a microcode unit in a microprocessor, for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit includes an instruction address input for receiving an instruction address, a control variable input for receiving a control variable corresponding to a current state of the microprocessor, a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction, and a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals *required* for executing said received instruction.

In another exemplary embodiment of the present invention, as defined by independent claim 20, a method of providing a state machine decoding includes decoding a current opcode to provide a decode, setting required functions signals, setting exclusive functions outside of the current opcode to a previous state; and latching results of the decode.

In the claimed invention, in addition to the "0" or "1" value which can be set for each control signal, the previous value can also be set, thereby reducing the power within the microprocessor (e.g., see specification at page 10, lines 2-5).

Specifically, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely required for that particular microcode address

(e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized since node toggle, as discussed above, is greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11).

For example, in an exemplary embodiment of the claimed invention, the power savings was on the order of about 30-40% over the conventional systems. Hence, if the function remains the same from a previous opcode to the next opcode (and hence from cycle-to-cycle), then the previous value may be maintained again, and no node toggle results since values are not being changed from high to low or from low to high (e.g., see specification at page 10, lines 11-16).

Thus, with the claimed invention, each opcode becomes a function of the previous opcode and only conflicting (e.g., required) control signals must be resolved, thereby greatly reducing power consumption (e.g., see specification at page 10, lines 17-19).

II. THE PRIOR ART REJECTIONS

A. Claim 20 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Damouny.

Applicants respectfully disagree with the Examiner's position for the following reasons, and therefore, respectfully traverse this rejection.

For example, claim 20 recites, *inter alia*, a method of providing a state machine decoding, comprising:

> decoding a current opcode to provide a decode;
> setting required functions signals;
> setting exclusive functions outside of the current opcode to a previous state; and
> latching results of the decode (emphasis added).

The Office Action alleges that Damouny discloses a method of providing a state machine decoding including setting required functions signals, as claimed. Particularly, the Examiner alleges that Damouny discloses that the pointers are necessary for execution and thus are required functions signals (see Office Action at page 3, numbered paragraph 7; emphasis added).

However, Applicants respectfully submit that the Examiner is mischaracterizing the Damouny reference.

That is, disclosing generally that the pointers are necessary for execution does not mean that Damouny discloses or suggests setting only the required function signals, as claimed.

On the contrary, Damouny does not disclose, suggest, or even contemplate *which* of the function signals would be set. Indeed, Damouny does not disclose, suggest, or even address the problems being solved by the claimed invention.

In comparison, the claimed invention discloses that, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely *required* for that particular microcode address (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized and node toggle can be greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11).

For at least the foregoing reasons, Applicants respectfully submit that Damouny neither discloses nor suggests all of the features of independent claim 20, and therefore, respectfully request that the Examiner withdraw this rejection and permit claim 20 to pass to immediate allowance.

B. Claims 1-4, 6, and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Damouny in view of Thoma.

Applicants respectfully submit that neither Damouny nor Thoma, either alone or in combination, discloses or suggests all of the features of the claimed invention.

Applicants respectfully submit that it would not have been obvious to combine Damouny and Thoma to arrive at the claimed invention, and even if combined, the combination of Damouny and Thoma still would not have arrived at the claimed invention.

For example, as mentioned above, the claimed invention provides a novel and unique combination of elements in which, in addition to the "0" or "1" value which can be set for each control signal, the previous value can also be set, thereby reducing the power within the microprocessor (e.g., see specification at page 10, lines 2-5).

Specifically, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely required for that particular microcode address (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized since node toggle, as discussed above, is greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11).

That is, in an exemplary embodiment of the claimed invention, each opcode becomes a function of the previous opcode and only conflicting (e.g., required) control signals must be resolved, thereby greatly reducing power consumption (e.g., see specification at page 10, lines 17-19).

Applicants respectfully submit that neither Damouny nor Thoma, either alone or in combination, discloses, suggests, or even contemplates these features of the claimed invention, or the advantages derived therefrom.

Moreover, Applicants respectfully submit that neither Damouny nor Thoma, either alone or in combination, discloses, suggests, or even contemplates *which* of the function signals would be set. Indeed, neither Damouny nor Thoma discloses, suggests, or even addresses the problems being solved by the claimed invention.

In comparison, the claimed invention discloses that, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely *required* for that particular microcode address (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized and node toggle can be greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11).

For example, independent claim 1 recites, *inter alia*, a microprocessor, comprising:

> a microcode unit for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:
>
> an instruction address input for receiving an instruction address;
>
> a control variable input for receiving a control variable corresponding to a current state of the microprocessor;
>
> a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; and
>
> a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing said received instruction (emphasis added).

Applicants respectfully submit that neither Damouny nor Thoma, either alone or in combination, discloses, suggests, or even contemplates these features of independent claim 1, and therefore, the Examiner respectfully is requested to withdraw this rejection.

Independent claim 9 recites somewhat similar features as independent claim 1, and therefore, Applicants respectfully submit that claim 9 also is patentable over Damouny and Thoma, either alone or in combination, for somewhat similar reasons as independent claim 1.

Moreover, dependent claims 2-4 and 6 also should be patentable at least by virtue of their dependency from claim 1, as well as for the additional recitations recited therein.

For example, claim 2 recites, *inter alia*, that each of the embedded logic circuits includes:

> a table for performing a table lookup in response to a received instruction; and
> wherein said controller is responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup for controllably setting each of the control signals *required* by the microprocessor for executing said received instruction (emphasis added).

The Examiner alleges that, as shown in Figure 1A, the branch PLA's 180 are responsive to the control variable (element 184), the control signals for an immediately preceding instruction (element 182), and to the table lookup for setting the required control signals (element 183) (see Office Action at pages 6-7, numbered paragraph 11).

However, Damouny does not disclose or suggest that the controller is responsive to: (1) the control variable, (2) the control signals for an immediately preceding instruction, and (3) to the table lookup for controllably setting each of the control signals *required* by the microprocessor for executing the received instruction.

That is, Damouny does not appear to distinguish between control signals required for executing the received instruction and those control signals that are not required for executing

the received instruction. Indeed, Damouny does not disclose, suggest, or even contemplate *which* of the function signals would be set, or for that matter, even addresses the problems being solved by the claimed invention.

For at least this reason, Applicants respectfully submit that dependent claim 2 is patentable over Damouny and Thoma, either alone or in combination, and therefore, the rejection of claim 2 should be withdrawn.

With respect to dependent claim 3, the Examiner alleges that "*[s]ince the limitations (a) and (b) of the claim state that this setting is regardless of the preceding value. the value may or may not be set based on the previous value and this portion of the limitations is not given weight and these two limitations are met*" (see Office Action at page 7, numbered paragraph 12; emphasis added). Applicants respectfully disagree.

For example, dependent claim 3 recites, *inter alia*, that the controller includes:

> means for setting a control signal to a "1" regardless of its immediately preceding value;
> means for setting a control signal to a "0" regardless of its immediately preceding value; and
> means for not modifying a control signal from its immediately preceding value (emphasis added).

The Examiner appears to allege that the "means for setting a control signal to a "1"..." and the "means for setting a control signal to a "0"..." somehow preclude a "means for not modifying a control signal..." as claimed, and therefore, does not give patentable weight to this recitation.

Applicants respectfully submit that the Examiner's position clearly is unreasonable.

Contrary, to the Examiner's position, claim 3 specifically recites each of these limitations and none of the stated limitations precludes another limitation.

That is, "means for setting a control signal to a "1"..." or "means for setting a control signal to a "0"..." does not mean that all control signals are set to "1" or all control signals are set to "0", such that the recited "means for not modifying a control signal..." would not be given patentable weight.

For example, the specification clearly describes that, in addition to the "0" or "1" value which can be set for each control signal, the previous value can also be set, thereby reducing the power within the microprocessor (e.g., see specification at page 10, lines 2-5).

Thus, contrary to the Examiner's position, the claimed "means for not modifying a control signal..." should have been given patentable weight.

For at least this reason, Applicants respectfully submit that claim 3 is patentable over Damouny and Thoma, either alone or in combination, and therefore, the rejection of claim 3 should be withdrawn.

On the other hand, dependent claim 6 recites, *inter alia*, "means for determining which of the control signals are not to be modified for each instruction" (emphasis added).

The Examiner alleges that, "*[s]ince the disclosure of Damouny is of a standard architecture where the control signals are set for each operation, every control signal is modified for each instruction, though some are modified at times to be the same value as a preceding signal. Thus it is determined that none of the control signals are to be not modified, since each signal is set.*" (see Office Action at page 8, numbered paragraph 14; emphasis added).

Applicants respectfully disagree.

As the Examiner apparently acknowledges, Damouny does not affirmatively and purposefully disclose that a determination is made (e.g., means for determining which of the

control signals are not to be modified for each instruction and which are to be modified for each instruction).

On the other hand, by merely disclosing that every control signal is modified for each instruction, Damouny clearly is not disclosing that a determination is made.

That is, Damouny clearly does not disclose any structure, equivalents thereof, or identity of function necessary for the claimed means for determining.

Instead, Damouny merely discloses that every control signal is modified for each instruction. In other words, modifying every control signal is automatic and no determination would need to be made.

Indeed, the Examiner has not identified any disclosure in Damouny to support that a determination is made.

Thus, Damouny clearly does not disclose or suggest any structure, equivalents thereof, or identity of function necessary for the claimed means for determining.

For at least these reasons, Applicants respectfully submit that neither Damouny nor Thoma, either alone or in combination, discloses or suggests all of the features of claim 6.

Therefore, Applicants respectfully request that the Examiner withdraw the rejection of claim 6 and permit this claim to pass to immediate allowance.

To summarize, for at least the foregoing reasons, Applicants respectfully submit that neither Damouny nor Thoma, either alone or in combination, discloses or suggests all of the features of claims 1-4, 6, and 9. Therefore, the Examiner respectfully is requested to withdraw the rejection of these claims and permit claims 1-4, 6, and 9 to pass to immediate allowance.

III. NEW CLAIMS

New claims 23-30 have been added to provide more varied protection for the present invention, as defined by the original specification and drawings.

Applicants submit that claims 23-30 are patentable over the cited references for somewhat similar reasons as those set forth above and respectfully requests allowance of the same.

IV. FORMAL MATTERS AND CONCLUSION

The Office Action objects to the drawings because all of the reference numerals allegedly are not recited in the specification. Applicants amend the specification to include reference numeral "S41".

However, with respect to reference numerals S42-S52, Applicants respectfully submit that these reference numerals are set forth in the specification (e.g., see specification at page 17, line 9, to page 19, line 10).

Thus, Applicants respectfully request that the Examiner withdraw this objection.

The Office Action also objects to the Title of the Invention. Applicants have amended the Title of the Invention herewith to indicate more clearly the invention to which the claims are directed, and therefore, respectfully request entry of the same and withdrawal of the objection.

In view of the foregoing, Applicants submit that claims 1-4, 6, 9, 20, and 23-30, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: July 16, 2004

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CERTIFICATE OF TRANSMISSION

I certify that I transmitted via facsimile to (703) 872-9306 the enclosed Amendment under 37 C.F.R. § 1.111 to Examiner Shane F. Gerstl on July 16, 2004.

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